HI-3593

3.3V ARINC 429 Dual Receiver, Single Transmitter with SPI Interface

July 2020

GENERAL DESCRIPTION

The HI-3593 from Holt Integrated Circuits is a CMOS integrated circuit for interfacing a Serial Peripheral Interface (SPI) enabled microcontroller to the ARINC 429 serial bus. The device provides two receivers, each with user-programmable label recognition for any combination of 256 possible labels, 32 x 32 Receive FIFO, 3 priority-label quick-access double-buffered registers and analog line receiver. The independent transmitter has a 32 x 32 Transmit FIFO and built-in line driver. The line driver operates from a single 3.3V supply and includes on-chip DC/DC converter to generate the bipolar ARINC 429 differential voltage levels needed to directly drive the ARINC 429 bus. The status of the transmit and receive FIFOs and priority-label buffers can be monitored using the programmable external interrupt pins, or by polling the HI-3593 Status Registers. Other features include a programmable option of data or parity in the 32nd bit, and the ability to switch the bit-significance of ARINC 429 labels. Pins are available with different input resistance and output resistance values which provides flexibility when using external lightning protection circuitry.

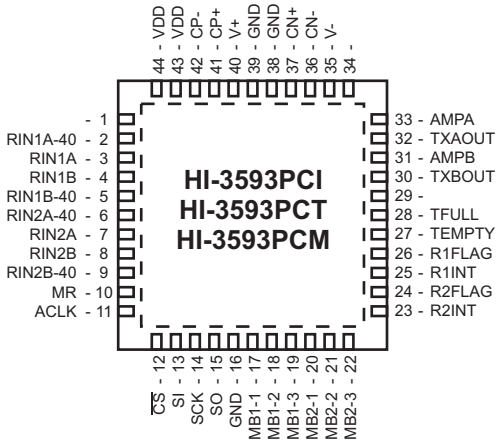
The Serial Peripheral Interface minimizes the number of host interface signals resulting in a small footprint device that can be interfaced to a wide range of industry-standard microcontrollers supporting SPI. Alternatively, the SPI signals may be controlled using just four general purpose I/O port pins from a microcontroller or custom FPGA. The SPI and all control signals are CMOS and TTL compatible and support 3.3V operation.

The HI-3593 applies the ARINC 429 protocol to the receivers and transmitter. ARINC 429 databus timing comes from a 1 MHz clock input, or an internal counter can derive it from higher clock frequencies having certain fixed values, possibly the external host processor clock.

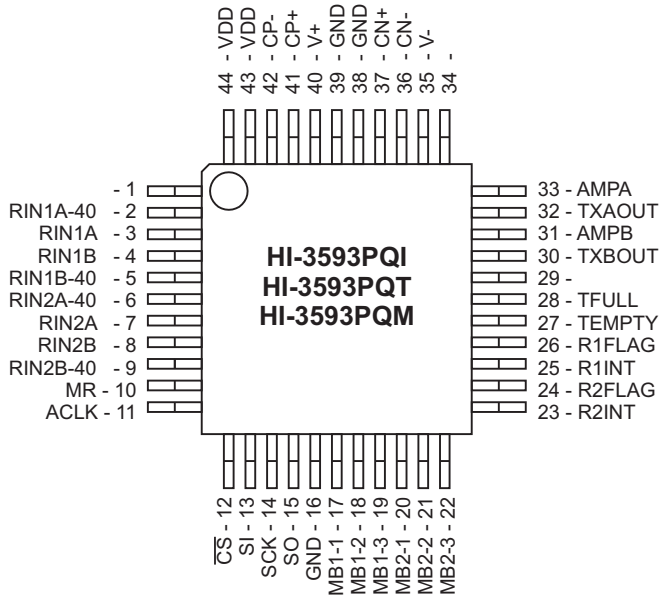
FEATURES

- ARINC 429 specification compliant
- Single 3.3V power supply
- On-chip analog line driver and receiver connect directly to ARINC 429 bus
- Programmable label recognition for 256 labels
- 32 x 32 Receive FIFOs and Priority-Label buffers
- Independent data rates for Transmit and Receive
- 10MHz, four-wire Serial Peripheral Interface (SPI)
- Industrial & extended temperature ranges

PIN CONFIGURATIONS (Top View)



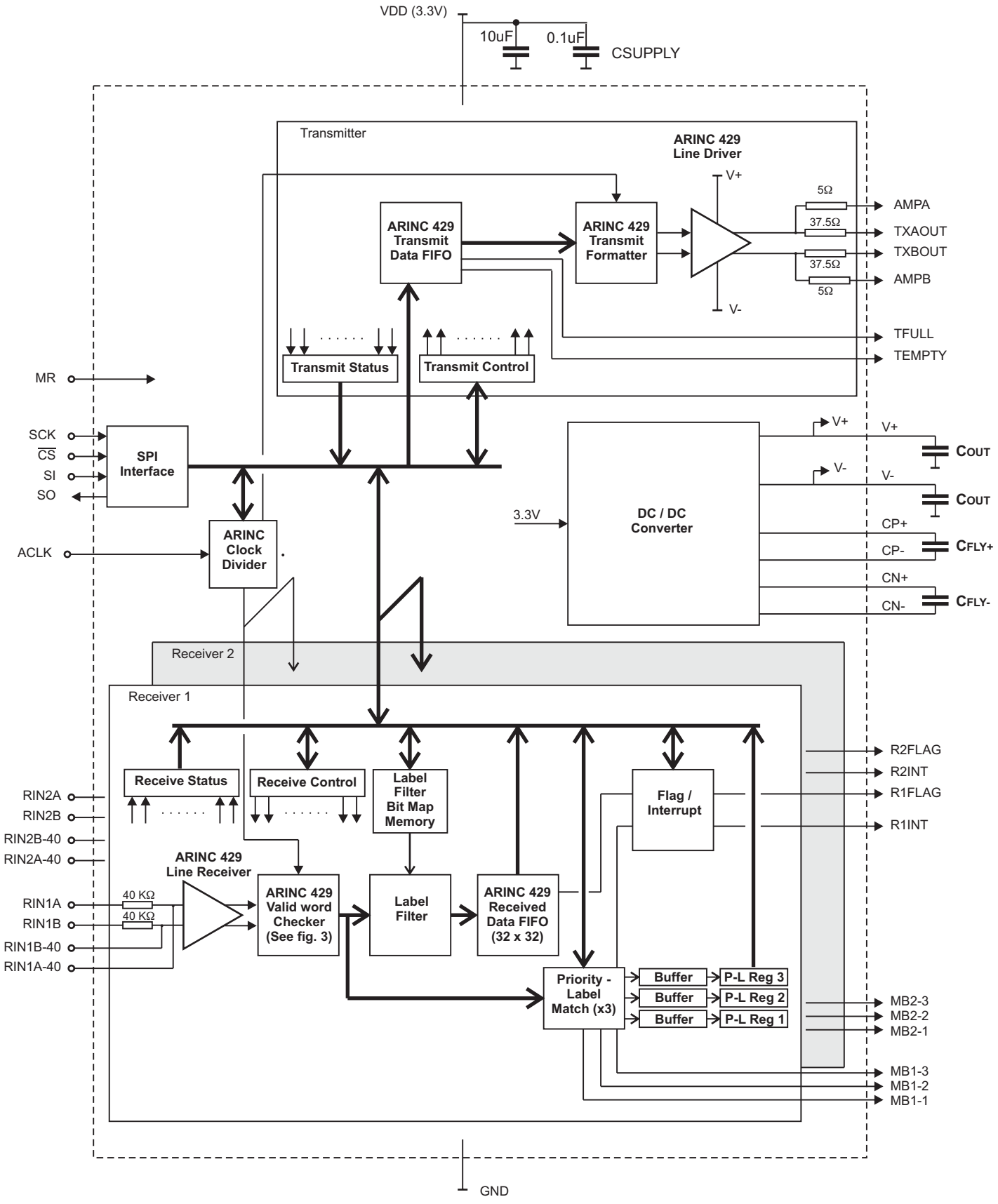
44 - Pin Plastic 7mm x 7mm Chip-Scale Package (QFN)



44 - Pin Plastic Quad Flat Pack (PQFP)

See page 18 for Additional Package Configurations

BLOCK DIAGRAM



PIN DESCRIPTIONS

SIGNAL	FUNCTION	DESCRIPTION	INTERNAL PULL UP / DOWN
RIN1A-40	INPUT	Alternate ARINC receiver 1 positive input. Requires external 40K ohm resistor	
RIN1A	INPUT	ARINC receiver 1 positive input. Direct connection to ARINC 429 bus	
RIN1B	INPUT	ARINC receiver 1 negative input. Direct connection to ARINC 429 bus	
RIN1B-40	INPUT	Alternate ARINC receiver 1 negative input. Requires external 40K ohm resistor	
RIN2A-40	INPUT	Alternate ARINC receiver 2 positive input. Requires external 40K ohm resistor	
RIN2A	INPUT	ARINC receiver 2 positive input. Direct connection to ARINC 429 bus	
RIN2B	INPUT	ARINC receiver 2 negative input. Direct connection to ARINC 429 bus	
RIN2B-40	INPUT	Alternate ARINC receiver 2 negative input. Requires external 40K ohm resistor	
MR	INPUT	Master Reset. A positive pulse clears Receive and Transmit data FIFOs and flags	50K ohm pull-down
ACLK	INPUT	Master timing source for the ARINC 429 receiver and transmitter	50K ohm pull-down
$\overline{CS}$	INPUT	Chip Select. Data is shifted into SI and out of SO when $\overline{CS}$ is low.	50K ohm pull-up
SI	INPUT	SPI interface serial data input	50K ohm pull-down
SCLK	INPUT	SPI Clock. Data is shifted into or out of the SPI interface using SCK	50K ohm pull-down
SO	OUTPUT	SPI interface serial data output	
GND	POWER	Chip 0V supply	
MB1-1	OUTPUT	Goes high when Receiver 1, Priority-Label Mail Box 1 contains a message	
MB1-2	OUTPUT	Goes high when Receiver 1, Priority-Label Mail Box 2 contains a message	
MB1-3	OUTPUT	Goes high when Receiver 1, Priority-Label Mail Box 3 contains a message	
MB2-1	OUTPUT	Goes high when Receiver 2, Priority-Label Mail Box 1 contains a message	
MB2-2	OUTPUT	Goes high when Receiver 2, Priority-Label Mail Box 2 contains a message	
MB2-3	OUTPUT	Goes high when Receiver 2, Priority-Label Mail Box 3 contains a message	
R2INT	OUTPUT	Receiver 2 programmable Interrupt pin	
R2FLAG	OUTPUT	Goes high as defined by Flag / Interrupt Assignment Register	
R1INT	OUTPUT	Receiver 1 programmable Interrupt pin	
R1FLAG	OUTPUT	Goes high as defined by Flag / Interrupt Assignment Register	
TEMPTY	OUTPUT	Goes high when the Transmit FIFO is empty	
TFULL	OUTPUT	Goes high when the Transmit FIFO contains the maximum 32 ARINC 429 words	
TXBOUT	OUTPUT	ARINC line driver negative output. Direct connection to ARINC 429 bus	
AMPB	OUTPUT	Alternate ARINC line driver negative output. Requires external 32.5 ohm resistor	
TXAOUT	OUTPUT	ARINC line driver positive output. Direct connection to ARINC 429 bus	
AMPA	OUTPUT	Alternate ARINC line driver positive output. Requires external 32.5 ohm resistor	
V-	CONVERTER	DC/DC negative voltage output	
CN-	CONVERTER	DC/DC converter fly capacitor for V-	
CN+	CONVERTER	DC/DC converter fly capacitor for V-	
V+	CONVERTER	DC/DC positive voltage output	
CP-	CONVERTER	DC/DC converter fly capacitor for V+	
CP+	CONVERTER	DC/DC converter fly capacitor for V+	
VDD	POWER	Chip 3.3V supply	

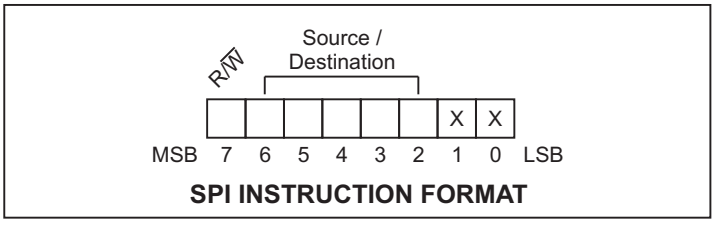
INSTRUCTIONS

Instruction op codes are used to read, write and configure the HI-3593. When $\overline{CS}$ goes low, the next 8 clocks at the SCK pin shift an instruction op code into the decoder, starting with the first rising edge. The op code is fed into the SI pin, most significant bit first.

For write instructions, the most significant bit of the data word must immediately follow the instruction op code and is clocked into its register on the next rising SCK edge. Data word length varies depending on word type written: 8-bit Control Register writes, 32-bit ARINC label writes or 256-bit writes to a channel's label-matching enable/disable memory.

For read instructions, the most significant bit of the requested data word appears at the SO pin after the last op code bit is clocked into the decoder, at the next falling SCK edge. As in write instructions, the data field bit-length varies with read instruction type.

SPI Instructions are of a common format. The first bit specifies whether the instruction is a write "0" or read "1" transfer. The next five bits specify the source or destination of the associated data byte(s), and the last two bits are "don't care".



SPI INSTRUCTION FORMAT

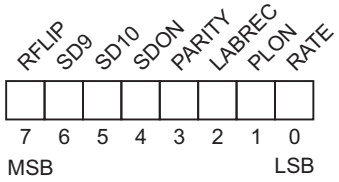
TABLE 1. DEFINED INSTRUCTIONS

Op-Code	R/W	# Data bytes	DESCRIPTION
0x00	W	0	Instruction not implemented. No operation.
0x04	W	0	Software controlled Master Reset
0x08	W	1	Write Transmit Control Register
0x0C	W	4	Write ARINC 429 message to Transmit FIFO
0x10	W	1	Write Receiver 1 Control Register
0x14	W	32	Write label values to Receiver 1 label memory. Starting with label 0xFF, consecutively set or reset each label in descending order. For example, if the first data byte is programmed to 10110010 then labels FF, FD FC and F9 will be set and FE, FB, FA and F8 will be reset.
0x18	W	3	Write Receiver 1 Priority-Label Match Registers. The data field consists of three eight-bit labels. The first data byte is written to P-L filter #3, the second to P-L filter #2, and the last byte to filter #1
0x24	W	1	Write Receiver 2 Control Register
0x28	W	32	Write label values to Receiver 2 label memory. Starting with label 0xFF, consecutively set or reset each label in descending order. For example, if the first data byte is programmed to 10110010 then labels FF, FD FC and F9 will be set and FE, FB, FA and F8 will be reset.
0x2C	W	3	Write Receiver 2 Priority-Label Match Registers. The data field consists of three eight-bit labels. The first eight bits is written to P-L filter #3, the second to P-L filter #2, and the last byte to filter #1
0x34	W	1	Write Flag / Interrupt Assignment Register
0x38	W	1	Write ACLK Division Register
0x40	W	0	Transmit current contents of Transmit FIFO if Transmit Control Register bit 5 (TMODE) is a “0”
0x44	W	0	Software Reset. Clears the Transmit and Receive FIFOs and the Priority-Label Registers
0x48	W	0	Set all bits in Receiver 1 label memory to a “1”
0x4C	W	0	Set all bits in Receiver 2 label memory to a “1”
0x80	R	1	Read Transmit Status Register
0x84	R	1	Read Transmit Control Register
0x90	R	1	Read Receiver 1 Status Register
0x94	R	1	Read Receiver 1 Control Register
0x98	R	32	Read label values from Receiver 1 label memory.
0x9C	R	3	Read Receiver 1 Priority-Label Match Registers.
0xA0	R	4	Read one ARINC 429 message from the Receiver 1 FIFO
0xA4	R	3	Read Receiver 1 Priority-Label Register #1, ARINC429 bytes 2,3 & 4 (bits 9 - 32)
0xA8	R	3	Read Receiver 1 Priority-Label Register #2, ARINC429 bytes 2,3 & 4 (bits 9 - 32)
0xAC	R	3	Read Receiver 1 Priority-Label Register #3, ARINC429 bytes 2,3 & 4 (bits 9 - 32)
0xB0	R	1	Read Receiver 2 Status Register
0xB4	R	1	Read Receiver 2 Control Register
0xB8	R	32	Read label values from Receiver 2 label memory.
0xBC	R	3	Read Receiver 2 Priority-Label Match Registers.
0xC0	R	4	Read one ARINC 429 message from the Receiver 2 FIFO
0xC4	R	3	Read Receiver 2 Priority-Label Register #1, ARINC429 bytes 2,3 & 4 (bits 9 - 32)
0xC8	R	3	Read Receiver 2 Priority-Label Register #2, ARINC429 bytes 2,3 & 4 (bits 9 - 32)
0xCC	R	3	Read Receiver 2 Priority-Label Register #3, ARINC429 bytes 2,3 & 4 (bits 9 - 32)
0xD0	R	1	Read Flag / Interrupt Assignment Register
0xD4	R	1	Read ACLK Division Register
0xFF	R	0	Instruction not implemented. No operation.

REGISTER DESCRIPTIONS

RECEIVE CONTROL REGISTER

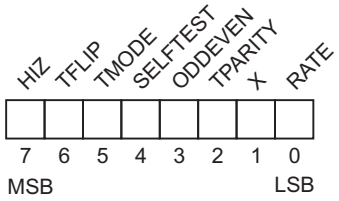
(Receiver 1 Write, SPI Op-code 0x10)
(Receiver 1 Read, SPI Op-code 0x94)
(Receiver 2 Write, SPI Op-code 0x24)
(Receiver 2 Read, SPI Op-code 0xB4)



Bit	Name	R/W	Default	Description
7	RFLIP	R/W	0	Setting this bit reverses the bit order of the first 8 bits of each ARINC 429 message received. See figure 1 for details.
6	SD9	R/W	0	If the receiver decoder is enable by setting the SDON bit to a “1”, then ARINC 429 message bit 9 must match this bit for the message to be accepted.
5	SD10	R/W	0	If the receiver decoder is enable by setting the SDON bit to a “1”, then ARINC 429 message bit 10 must match this bit for the message to be accepted.
4	SDON	R/W	0	If this bit is set, bits 9 and 10 of the received ARINC 429 message must match SD9 and SD10
3	PARITY	R/W	0	Received word parity checking is enabled when this bit is set. If “0”, all 32 bits of the received ARINC 429 word are stored without parity checking.
2	LABREC	R/W	0	When “0”, all received messages are stored. If this bit is set, incoming ARINC message label filtering is enabled. Only messages whose corresponding label filter table entry is set to a “1” will be stored in the Receive FIFO.
1	PLON	R/W	0	Priority-Label Register enable. If PLON = “1” the three Priority-Label Registers are enabled and received ARINC 429 messages with labels that match one of the three pre-programmed values will be capured and stored in the corresponding Prioty-Label Mail Boxes. If PLON = “0” the Priority-Label matching feature is turned off and no words are placed in the mail boxes.
0	RATE	R/W	0	If RATE is “0”, ARINC 429 high-speed data rate is selected. RATE = “1” selects low-speed ARINC 429 data rate (high-speed / 8).

TRANSMIT CONTROL REGISTER

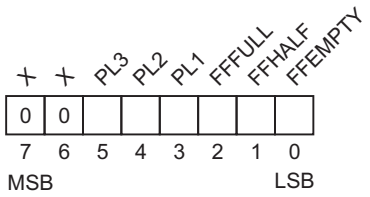
(Write, SPI Op-code 0x08)
(Read, SPI Op-code 0x84)



Bit	Name	R/W	Default	Description
7	HIZ	R/W	0	Setting this bit puts the on-chip line driver outputs to a high-impedance state.
6	TFLIP	R/W	0	Setting this bit reverses the bit order of the first 8 bits of each ARINC 429 message transmitted. See figure 1 for details.
5	TMODE	R/W	0	If TMODE is “0”, data in the transmit FIFO is sent to the ARINC 429 bus only upon receipt of an SPI op-code 0x40, transmit enable, command. If TMODE is a “1”, data is sent as soon as it is available.
4	SELFTEST	R/W	0	Setting SELFTEST causes an internal connection to be made looping-back the transmitter outputs to both receiver inputs for self-test purposes. When in self-test mode, the HI-3593 ignores data received on the two ARINC 429 receive channels and holds the on-chip line driver outputs in the NULL state to prevent self-test data being transmitted to other receivers on the bus.
3	ODDEVEN	R/W	0	If the TPARITY bit is set, the transmitter inserts an odd parity bit if ODDEVEN = “0”, or an even if ODDEVEN = “1”.
2	TPARITY	R/W	0	If TPARITY = “0”, no parity bit is inserted and the 32nd transmitted bit is data. When TPARITY is a “1” a parity bit is substituted for bit 32 according to the ODDEVEN bit value.
1	X	R/W	0	Not used.
0	RATE	R/W	0	If RATE is “0”, ARINC 429 high-speed data rate is selected. RATE = “1” selects low-speed ARINC 429 data rate (high-speed / 8).

RECEIVE STATUS REGISTER

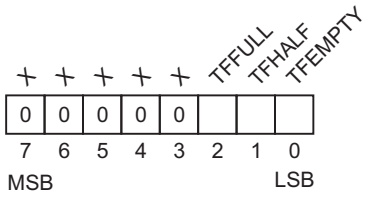
(Receiver 1 Read, SPI Op-code 0x90)
(Receiver 2 Read, SPI Op-code 0xB0)



Bit	Name	R/W	Default	Description
7	X	R	0	Not used. Always reads "0"
6	X	R	0	Not used. Always reads "0"
5	PL3	R	0	This bit is set when a message is received by Priority Label filter #3
4	PL2	R	0	This bit is set when a message is received by Priority Label filter #2
3	PL1	R	0	This bit is set when a message is received by Priority Label filter #1
2	FFFULL	R	0	This bit is set when the Receive FIFO contains 32 ARINC 429 messages
1	FFHALF	R	0	This bit is set when the Receive FIFO contains at least 16 ARINC 429 messages
0	FFEMPTY	R	1	This bit is set when the Receive FIFO is empty

TRANSMIT STATUS REGISTER

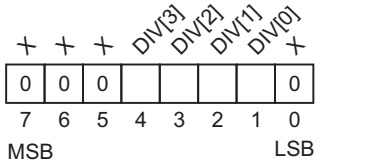
(Read, SPI Op-code 0x80)



Bit	Name	R/W	Default	Description
7	X	R	0	Not used. Always reads "0"
6	X	R	0	Not used. Always reads "0"
5	X	R	0	Not used. Always reads "0"
4	X	R	0	Not used. Always reads "0"
3	X	R	0	Not used. Always reads "0"
2	TFFULL	R	0	This bit is set when the Transmit FIFO contains 32 ARINC 429 messages
1	TFHALF	R	0	This bit is set when the Transmit FIFO contains at least 16 ARINC 429 messages
0	TFEMPTY	R	1	This bit is set when the Transmit FIFO is empty

ACLK DIVISION REGISTER

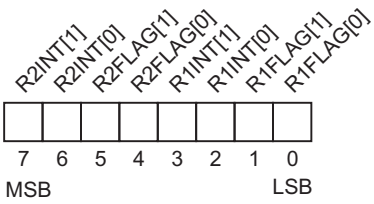
(Write, SPI Op-code 0x38)
(Read, SPI Op-code 0xD4)



Bit	Name	R/W	Default	Description
7	X	R/W	0	Not used.
6	X	R/W	0	Not used.
5	X	R/W	0	Not used.
4 - 1	DIV[3:0]	R/W	0	The value programmed in DIV[3:0] sets the ACLK division ratio (see table 2)
0	X	R/W	0	Not used.

FLAG / INTERRUPT ASSIGNMENT REGISTER

(Write, SPI Op-code 0x34)
(Read, SPI Op-code 0xD0)



Bit	Name	R/W	Default	Description
7-6	R2INT[1:0]	R/W	0	The value of R2INT[1:0] defines the function of the R2INT output pin, as follows: 00 R2INT pulses high when a valid message is received and placed in the Receiver 2 FIFO or any of the Receiver 2 Priority-Label mail boxes 01 R2INT pulses high when a message is received in Receiver 2 Priority-Label mail box #1 10 R2INT pulses high when a message is received in Receiver 2 Priority-Label mail box #2 11 R2INT pulses high when a message is received in Receiver 2 Priority-Label mail box #3
5-4	R2FLAG[1:0]	R/W	0	The value of R2FLAG[1:0] defines the function of the R2FLAG output pin, as follows: 00 R2FLAG goes high when Receiver 2 FIFO is empty 01 R2FLAG goes high when Receiver 2 FIFO contains 32 ARINC 429 words (FIFO is full) 10 R2FLAG goes high when Receiver 2 FIFO contains at least sixteen ARINC 429 words (FIFO is half-full) 11 R2FLAG goes high when Receiver 2 FIFO contains one or more words (FIFO is not empty)
3-2	R1INT[1:0]	R/W	0	The value of R1INT[1:0] defines the function of the R1INT output pin, as follows: 00 R1INT pulses high when a valid message is received and placed in the Receiver 1 FIFO or any of the Receiver 1 Priority-Label mail boxes 01 R1INT pulses high when a message is received in Receiver 1 Priority-Label mail box #1 10 R1INT pulses high when a message is received in Receiver 1 Priority-Label mail box #2 11 R1INT pulses high when a message is received in Receiver 1 Priority-Label mail box #3
1-0	R1FLAG[1:0]	R/W	0	The value of R1FLAG[1:0] defines the function of the R1FLAG output pin, as follows: 00 R1FLAG goes high when Receiver 1 FIFO is empty 01 R1FLAG goes high when Receiver 1 FIFO contains 32 ARINC 429 words (FIFO is full) 10 R1FLAG goes high when Receiver 1 FIFO contains at least sixteen ARINC 429 words (FIFO is half-full) 11 R1FLAG goes high when Receiver 1 FIFO contains one or more words (FIFO is not empty)

ARINC 429 BIT ORDERING

ARINC 429 messages consist of a 32-bit sequence as shown below. The first eight bits that appear on the ARINC 429 bus are the label byte. The next twenty three bits comprise a data field which presents data in a variety of formats defined in the ARINC 429 specification. The last bit transmitted is an odd parity bit.

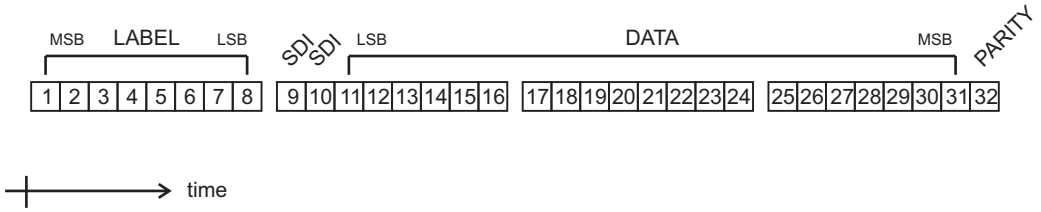
ARINC 429 data is transmitted between the HI-3593 and host microcontroller using the four-wire Serial Peripheral Interface (SPI). A read or write operation consists of a single-byte op-code followed by the data. When writing to the transmit FIFO or reading from the receive FIFOs, the SPI data field is four bytes. Figure 1 shows how the SPI data bytes are mapped to the ARINC 429 message.

ARINC 429 specifies the MSB of the label as ARINC bit 1. Conversely, the data field MSB is bit 31. So the bit significance of the label byte and data fields are opposite.

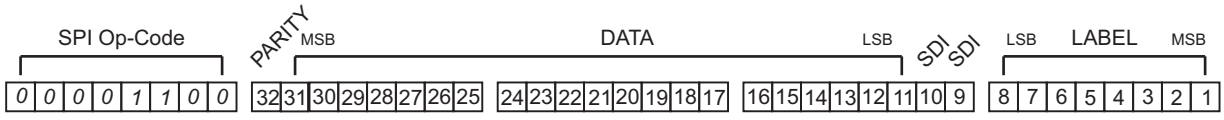
The HI-3593 may be programmed to “flip” the bit ordering of the label byte as soon as it is received and immediately prior to transmission. This is accomplished by setting the TFLIP bit to a “1” in the Transmit Control Register and/or the RFLIP bit in the Receive Control Registers. The RFLIP bit does not control Priority Label Match Registers.

Note that when reading ARINC 429 messages from the Priority-Label Registers the label byte is omitted to permit a faster read time. The label value will match the value loaded into the Match Register and therefore does not need to be output each time a message is read.

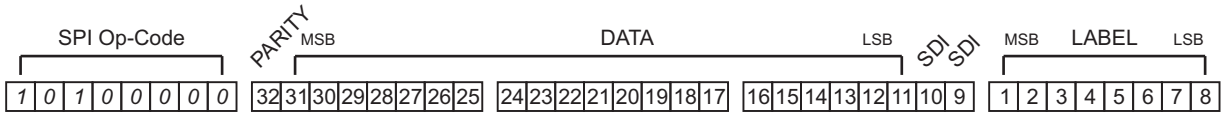
ARINC 429 Message as received / transmitted on the ARINC 429 serial bus



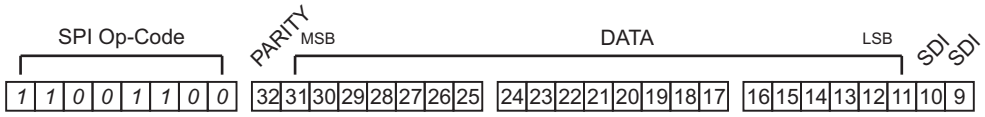
ARINC 429 Message as transferred on the SPI bus



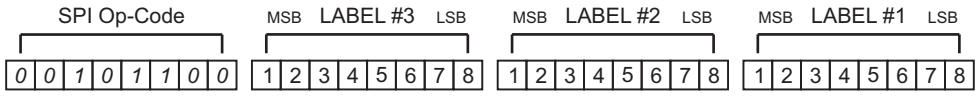
Example 1. Write Transmit FIFO (Op-Code 0x0C) with TFLIP bit = “0”.



Example 2. Read Receiver 1 FIFO (Op-Code 0xA0) with RFLIP bit = “1”.



Example 3. Read Receiver 2 Priority-Label Register #3 (Op-Code 0xCC).



Example 4. Write Receiver 2 Priority-Label Match Registers (Op-Code 0x2C)with RFLIP bit = “1” or “0”.

FIGURE 1. ARINC 429 & SPI BIT ORDERING

FUNCTIONAL DESCRIPTION

INITIALIZATION

The HI-3593 may be initialized using the Master Reset (MR) pin or under software control by executing SPI op-code 0x04. MR must be pulsed high for 1 µs to bring the part to its completely reset state. MR clears all three FIFOs, all six Priority-Label Mail Boxes, clears the Filter memories and Match registers and sets all other internal registers to their default state.

Software Reset is performed using SPI op-code 0x44. Software Reset clears all three FIFOs and all six Priority-Label Mail Boxes, but does not affect the values stored in the filter memories, Priority-Label Match registers or other writeable registers. The Transmit and Receive Status Registers will reflect the state of the post-software reset device.

CLOCK FREQUENCY SELECTION

For correct ARINC 429 data rate transmission and reception, and bit timing, the HI-3593 transmit and receive logic requires a 1 MHz +/- 1% reference clock source. The clock is input at the ACLK pin and must be 1 MHz or any even multiple of 1 MHz up to 30 MHz. If a clock source greater than 1 MHz is used, then the ACLK Division Register must be programmed with the appropriate scaling value.

Note that the least significant bit of the ACLK Division Register is fixed at “0” allowing only even numbers to be programmed. Similarly the three most significant bits are also fixed at “0” limiting the maximum value to 0x1E. The ACLK Division Register is cleared to 0x00 after Master Reset and is unaffected by Software Reset. When programmed to 0x00, the ACLK division ratio is one, and a 1 MHz clock should be applied to ACLK. The ACLK Division Register is loaded using SPI Op-Code 0x38 and read using Op-Code 0xD4.

The following table provides examples of ACLK frequency and ACLK Division Register values for correct ARINC 429 operation:

ACLK Division Register value	External Clock
0x00	1 MHz
0x02	2 MHz
0x04	4 MHz
0x06	6 MHz
0x08	8 MHz
0x0A	10 MHz
“	“
“	“
0x1C	28 MHz
0x1E	30 MHz

TABLE 2. ACLK DIVISION

CONFIGURATION

The Transmit Control Register and Receiver Control Registers are used to configure the ARINC 429 transmission channel and two ARINC 429 receive channels. The registers may be written or read at any time. They are reset to 0x00 following Master Reset and are unchanged by Software Reset. Refer to the Receiver Control Register and Transmit Control Register descriptions for detailed information.

ARINC 429 RECEIVERS

The HI-3593 has two completely independent ARINC 429 receive channels. Each channel has an on-chip analog line receiver for connection to the ARINC 429 incoming data bus. The ARINC 429 specification requires the following detection levels:

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5 Volts to +13 Volts
NULL	+2.5 Volts to -2.5 Volts
ZERO	-6.5 Volts to -13 Volts

The HI-3593 guarantees recognition of these levels with a common mode voltage with respect to GND less than ±30V for the worst case condition (3.15V supply and 13V signal level).

Design tolerances guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the ARINC signal (including nulls) is outside the differential voltage ranges, the HI-3593 receiver rejects the data.

BIT TIMING

The ARINC 429 specification defines the following timing tolerances for received data:

	HIGH SPEED (RATE = “0”)	LOW SPEED (RATE = “1”)
BIT RATE	100K BPS ± 1%	12K -14.5K BPS
PULSE RISE TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSE FALL TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSE WIDTH	5 µsec ± 5%	34.5 to 41.7 µsec

The HI-3593 accepts signals within these tolerances and rejects signals outside these tolerances. Receiver logic achieves this as described below:

1. An accurate 1MHz clock source is required to validate the receive signal timing.

2. The receiver uses three separate 10-bit sampling shift registers for Ones detection, Zeros detection and Null detection. When the input signal is within the differential voltage range for any shift register’s state (One, Zero or Null) sampling clocks a “1” into that register. When the receive signal is outside the differential voltage range defined for any shift register, a “0” is clocked. Only one shift register can clock a “1” for any given sample. All three registers clock zeros if the differential input voltage is between defined state voltage bands.

Valid data bits require at least three consecutive One or Zero samples (three “1’s”) in the first five positions of the Ones or Zeros sampling shift register, and at least three consecutive Null samples (three “1’s”) in the second five positions of the Null sampling shift register within the data bit interval.

A word gap Null requires at least three consecutive Null samples in the first half of the Null sampling shift register and at least three consecutive Null samples in the second half of the Null sampling shift register. This guarantees the minimum pulse width.

FUNCTIONAL DESCRIPTION (cont.)

3. To validate the receive data bit rate, each bit must follow its preceding bit by not less than 8 samples and not more than 12 samples. With exactly 1MHz input clock frequency, the acceptable data bit rates are:

	HIGH SPEED	LOW SPEED
DATA BIT RATE MIN	83K BPS	10.4K BPS
DATA BIT RATE MAX	125K BPS	15.6K BPS

4. Following the last data bit of a valid reception, the Word Gap timer samples the Null shift register every 10 input clocks (every 80 clocks for low speed). If a Null is present, the Word Gap counter is incremented. A Word Gap count of 3 enables the next reception.

RECEIVER PARITY

Receiver parity checking is enabled by setting the Receive Control register PARITY bit to a “1”. When enabled, the receiver parity circuit counts Ones received, including the parity bit. If the result is odd, a "0" is stored in the 32nd bit position, overwriting the received parity bit. The “0” indicates a parity bit check pass.

If receive parity is enabled and a word is received with bad odd parity, the 32nd bit is overwritten with a “1” indicating a parity check fail.

When the Receiver Control Register PARITY bit is a “0”, no parity checking takes place and all 32 bits of the received word remain unaltered.

RECEIVED DATA ACCEPTANCE AND STORAGE

The HI-3593 subjects incoming ARINC 429 messages to three different data filter checks before data is accepted. First all words are filtered for matching S/D bits, if enabled. Secondly, the word label byte must match one of the three programmed Priority-Label Match Register Values for the word to be stored in a Priority-Label Register, and/or the label memory filter bit corresponding to the label must be set to a “1” for the word to be stored in the Receiver FIFO.

S/D FILTERING

S/D filtering is enabled by setting the Receive Control Register SDON bit to a “1”. When enabled, bits 9 and 10 of the incoming ARINC 429 word are compared with Receive Control Register bits SD9 and SD10. If they match, the word is accepted for the next phase of filtering. If the bits do not match, the word is discarded and never stored. The S/D filtering function may be disabled by programming the SDON bit to a “0”. When disbled, all incoming words are accepted for subsequent filtering.

PRIORITY LABELS

The three Priority Label Registers store received data if the Priority Label feature is enabled, and the incoming ARINC 429 word’s label byte matches the value stored in Pririty-Label Match Register #1, # 2 or #3.

Priority-Label capture is enabled by setting the Receive Control Register PLON bit to “1”. When PLON = “0” the Priority-Label feature is disabled and no ARINC 429 words are stored in the Priority-Label Registers.

All three Priority-Label Match Registers are loaded using SPI op-code 0x18 (Receiver 1) or 0x2C (Receiver 2), followed by three label match values. The first byte is the match value for Priority-Label Register #3, the second for Priority-Label Register #2 and the third for Priority-Label #1. The match values may be checked by reading the Priority-Label Match Registers using SPI op-code 0x9C (Receiver 1) or 0xBC (Receiver 2).

When using the Priority-Label feature, all three Priority-Label Match Registers must be loaded to avoid unintended matches occurring on un-programmed Priority-Label Match Register random values. If less than three Priority-Labels are required for a particular application, duplicate copies of the same match value should be stored in two (or three) registers.

Note that Priority-Label Registers (mail boxes) are only 24 bits long. Because the ARINC 429 label byte value is pre-programmed for each register it is not necessary to store it when words are received. This allows a shorter and faster access of the data field using SPI Op-Codes 0xA4, 0xA8 and 0xAC (Receiver 1 Priority-Label Registers #1, #2 and #3) or 0xC4, 0xC8 and 0xCC (Receiver 2 Priority-Label Registers #1, #2 and #3).

The Receive Status Register bits PL1, PL2 and PL3 indicate when Priority-Label data is available in the Priority-Label Registers. Six status output pins MB1-1 through MB2-3 also indicate when data is available at each of the six Priority-Label Registers. The R1INT and R2INT interrupt pins can also be triggered when Priority Labels are captured by programming bits 7, 6, 3 and 2 of the Flag / Interrupt Assignment Register.

LABREC	ARINC word matches Enabled label	SDON	ARINC word bits 10, 9 match SD10, SD9	FIFO
0	X	0	X	Load FIFO
1	No	0	X	Ignore data
1	Yes	0	X	Load FIFO
0	X	1	No	Ignore data
0	X	1	Yes	Load FIFO
1	Yes	1	No	Ignore data
1	No	1	Yes	Ignore data
1	No	1	No	Ignore data
1	Yes	1	Yes	Load FIFO

TABLE 3. FIFO LOADING CONTROL

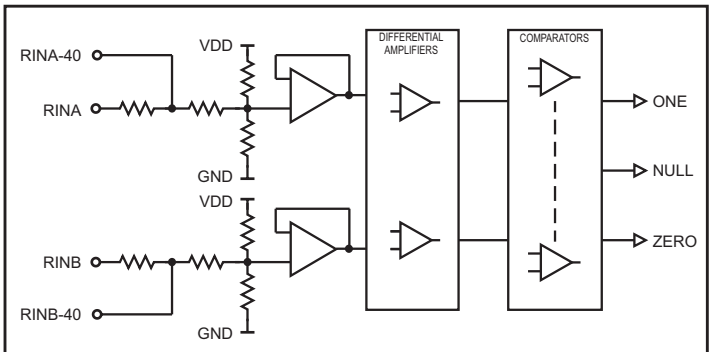


FIGURE 2. ARINC RECEIVER INPUT

FUNCTIONAL DESCRIPTION (cont.)

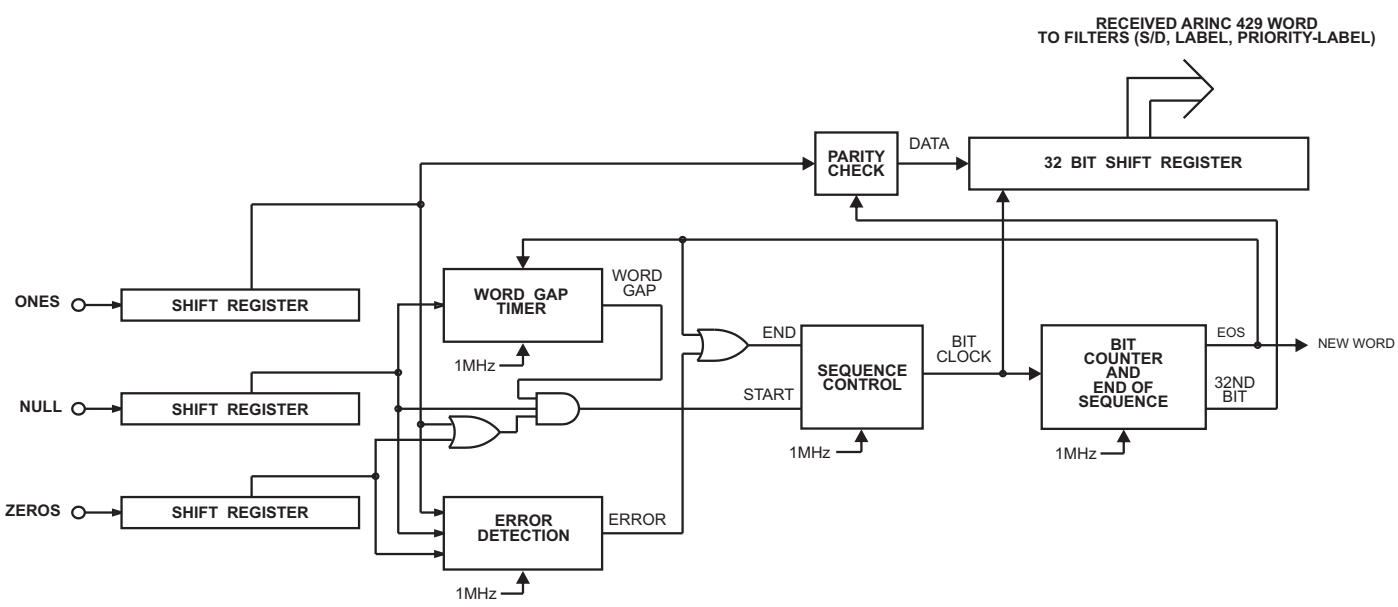


FIGURE 3. RECEIVER BLOCK DIAGRAM

RECEIVE DATA FIFO

Following S/D Filtering, accepted ARINC 429 words are conditionally stored in the Receive FIFO. If label filtering is disabled, all words are stored. If label filtering is enabled, the incoming ARINC429 word's label byte value is checked against its corresponding bit in the pre-programmed label look-up table. If the bit is set to a "1" the word is stored in the FIFO. If the bit is a "0" the word is not stored in the FIFO.

LABEL RECOGNITION

The user loads the 256-bit label look-up table to specify which 8-bit incoming ARINC labels are stored in the Receive FIFO, and which are not. Setting a "1" in the look-up table enables processing of received ARINC words containing the corresponding label. A "0" in the look-up table causes discard of received ARINC words containing the label. The 256-bit look-up table is loaded using SPI Op-Codes 0x14 (Receiver 1) and 0x28 (Receiver 2), as described in Table 1. After the look-up table is initialized, the Control Register bit LABREC must be set to enable label recognition.

All four bytes of the incoming ARINC429 word are stored in the FIFO.

Table 3. defines the rules for Receive FIFO loading.

READING THE LABEL LOOK-UP TABLE

The contents of the Label Look-up table may be read via the SPI interface using Op-Code 0x98 (Receiver 1) or 0xB8 (Receiver 2) as described in Table 1.

RETRIEVING DATA

Each time a valid ARINC 429 word is loaded into the FIFO, the Receive FIFO Status Register FFEMPTY, FFHALF and FFFULL bits are updated. When the FIFO is EMPTY, the FFEMPTY bit is a "1" and FFHALF and FFFULL are "0". Once the first received and accepted ARINC 429 word is loaded into the FIFO, FFEMPTY goes low. Each received ARINC 429 word is retrieved via the SPI interface using SPI Op-Code 0xA0 (Receiver 1) or 0xC0 (Receiver 2).

Up to 32 ARINC 429 words may be held in the Receive FIFO. FFFULL goes high when the Receive FIFO is full. Failure to unload the Receive FIFO when full causes additional valid ARINC 429 words to overwrite Receive FIFO location 32.

A FIFO half-full flag (FFHALF) is high whenever the Receive FIFO contains 16 or more words. The FFHALF bit provides a useful indicator to the host CPU that a sixteen word data retrieval routine may be performed.

The FFEMPTY, FFHALF or FFFULL status bits can also be output on the R1FLAG (Receiver 1) and R2FLAG (Receiver 2) pins. Flag / Interrupt Assignment Register bits 5, 4, 1 and 0 select which flag appears. Additionally, a FIFO not empty option may be programmed for the R1FLAG / R2FLAG pins causing the pin to go high any time at least one word is available in the FIFO.

FUNCTIONAL DESCRIPTION (cont.)

TRANSMITTER

FIFO OPERATION

Figure 4 shows a block diagram of the HI-3593 transmitter. The Transmit FIFO is loaded with ARINC 429 words awaiting transmission. SPI op-code 0x0C writes each ARINC 429 word into the FIFO, at the next available FIFO location. If Transmit Status Register bit TFEMPTY equals "1" (FIFO empty), then up to 32 words (32 bits each) may be loaded. If Transmit Status Register bit TFEMPTY equals "0" then only the available positions may be loaded. If all 32 positions are full, Transmit Status Register bit TFFULL is asserted. Further attempts to load the Transmit FIFO are ignored until at least one ARINC 429 word is transmitted.

The Transmit FIFO half-full flag (Transmit Status Register bit TFHALF) equals "0" when the Transmit FIFO contains less than 16 words. When TFHALF equals "0", the system microprocessor can safely initiate a 16-word ARINC 429 write sequence.

In normal operation (Transmit Control Register bit TPARITY = "1"), the 32nd bit transmitted is an odd parity bit. If Transmit Control Register bit PARITY equals "0", all 32 bits loaded into the Transmit FIFO are treated as data and are transmitted.

The Transmit and Receive FIFOs may be cleared using Software Reset (SPI op-code 0x44). The Transmit FIFO should be cleared after a self-test before starting normal operation to avoid inadvertent transmission of test data.

DATA TRANSMISSION

If Transmit Control Register bit TMODE equals "1", ARINC 429 data is transmitted immediately following the $\overline{CS}$ rising edge of the SPI instruction that loaded data into the Transmit FIFO. Writing Transmit Control Register bit TMODE to "0" allows the software to control transmission timing; each time an SPI op-code 0x40 is executed, all loaded Transmit FIFO words are transmitted. If new words are loaded into the Transmit FIFO before transmission stops, the new words will also be output. Once the Transmit FIFO is empty and transmission of the last word is complete, the FIFO can be loaded with new data which is held until the next SPI 0x40 instruction is executed. Once transmission is enabled, the FIFO positions are incremented with the top register loading into the data transmission shift register. Within 2.5 data clocks the first data bit appears at TXAOUT and TXBOUT. The 31 or 32 bits in the data transmission shift register are presented sequentially to the outputs in the ARINC 429 format with the following timing:

	HIGH SPEED	LOW SPEED
ARINC DATA BIT TIME	10 Clocks	80 Clocks
DATA BIT TIME	5 Clocks	40 Clocks
NULL BIT TIME	5 Clocks	40 Clocks
WORD GAP TIME	40 Clocks	320 Clocks

A word counter detects when all loaded positions have been transmitted and sets the Transmit Status Register TFEMPTY bit high.

TRANSMITTER PARITY

The parity generator counts the Ones in the 31-bit word. The 32nd bit transmitted will make parity odd. Setting Transmit Control Register bit TPARITY to "0" bypasses the parity generator, and allows 32 bits of data to be transmitted.

SELF TEST

If Transmit Control Register bit SELFTEST is equal "1", the transmitter serial output data is internally looped-back into the receiver 1. The data will appear inverted (compliment) on receiver 2. Data passes unmodified from transmitter to receiver 1. Setting Transmit Control register bit SELFTEST to "1" forces TXAOUT and TXBOUT to the Null state to prevent self-test data from appearing on the ARINC 429 bus.

SYSTEM OPERATION

The receivers are independent of the transmitter. Therefore, control of data exchanges is strictly at the option of the user. The only restrictions are:

1. The received data will be overwritten if the Receive FIFO is full and at least one location is not retrieved before the next complete ARINC 429 word is received.

2. The Transmit FIFO can store 32 words maximum and ignores attempts to load additional data when full.

DC/DC CONVERTER

The HI-3593 requires only a single +3.3V power supply. An integrated inverting / non-inverting voltage doubler generates the rail voltages (+/- 6.6V) which then power the line driver to produce the required +/- 5V ARINC 429 signal levels.

The internal dual-polarity charge pump requires four external capacitors, two for each polarity generated by the doubler. Pins CP+ and CP- connect the external "fly" capacitor, CFLY, to the positive portion of the doubler, resulting in twice VDD at the V+ pin. An output "hold" capacitor, COUT, is placed between V+ and GND. The inverting negative portion of the converter works in a similar fashion, with CFLY and COUT placed between CN+ / CN- and V- / GND respectively (see block diagram page 2). See Converter Characteristics table for recommended capacitor specifications.

LINE DRIVER OPERATION

The line driver in the HI-3593 directly drives the ARINC 429 bus. The two ARINC 429 outputs (TXAOUT and TXBOUT) provide a differential voltage to produce a +10V One, a -10V Zero, and a 0 Volt Null. Transmit Control Register bit RATE controls both the transmitter data rate and the slope of the differential output signal. No additional hardware is required to control the slope.

Writing Transmit Control Register bit RATE to "0" causes a 100 Kbit/s data rate and a slope of 1.5 µs on the ARINC 429 outputs. Setting RATE to "1" causes a 12.5 Kbit/s data rate and a slope of 10µs. Slope rate is set by an on-chip resistor and capacitor and tested to be within ARINC 429 specification requirements.

LINE DRIVER OUTPUT PINS

The HI-3593 TXAOUT and TXBOUT pins have 37.5 Ohms in series with each line driver output, and may be directly connected to an ARINC 429 bus. The alternate AMPA and AMPB pins have 5 Ohms of internal series resistance and require external 32.5 ohm resistors

FUNCTIONAL DESCRIPTION (cont.)

at each pin. AMPA and AMPB are for applications where external series resistance is applied, typically for lightning protection devices.

The line driver outputs TXAOUT, TXBOUT, AMPA and AMPB may be programmed to a high impedance state, allowing multiple line drivers to be connected to a single ARINC 429 bus. To tri-state the outputs bit HIZ in the Transmit Control Register must be programmed to a "1". Note that all other functions of the HI-3593 continue to operate as usual even though the outputs are tri-stated.

LINE RECEIVER INPUT PINS

The HI-3593 has two sets of Line Receiver input pins for each of the two receivers, RINxA/B and RINxA/B-40. Only one pair may be used to connect to the ARINC 429 bus. The unused pair must be left floating. The RINxA/B pins may be connected directly to the ARINC 429 bus. The RINxA/B-40 pins require external 40K ohm resistors in series with each ARINC input. These do not affect the ARINC receiver thresholds. By keeping excessive voltage outside the device, this option is helpful in applications where lightning protection is required.

When using the RINxA/B-40 pins, each side of the ARINC 429 bus must be connected through a 40K ohm series resistor in order for the chip to detect the correct ARINC 429 levels. The typical 10 Volt differential signal is translated and input to a window comparator and latch. The comparator levels are set so that with the external 40K ohm resistors, they are just below the standard 6.5 volt minimum ARINC 429 data threshold and just above the standard 2.5 volt maximum ARINC 429 null threshold.

Please refer to the Holt AN-300 Application Note for additional information and recommendations on lightning protection of Holt line drivers and line receivers.

MASTER RESET (MR)

Application of a Master Reset from the MR pin or execution of Opcode (0x04) causes immediate termination of data transmission and reception and clears the receive control registers, transmit control register, ACLK and Flag/Interrupt Registers to the default states. All FIFOs will be emptied and status flags are set to the default state (TFULL is reset, TEMPTY is set). **NOTE:** Reading an EMPTY FIFO may result in invalid data.

SOFTWARE RESET

Opcode (0x044) clears the transmit and receive FIFOs and the Priority-Label Registers **only.** All other registers are unaffected by Software Reset.

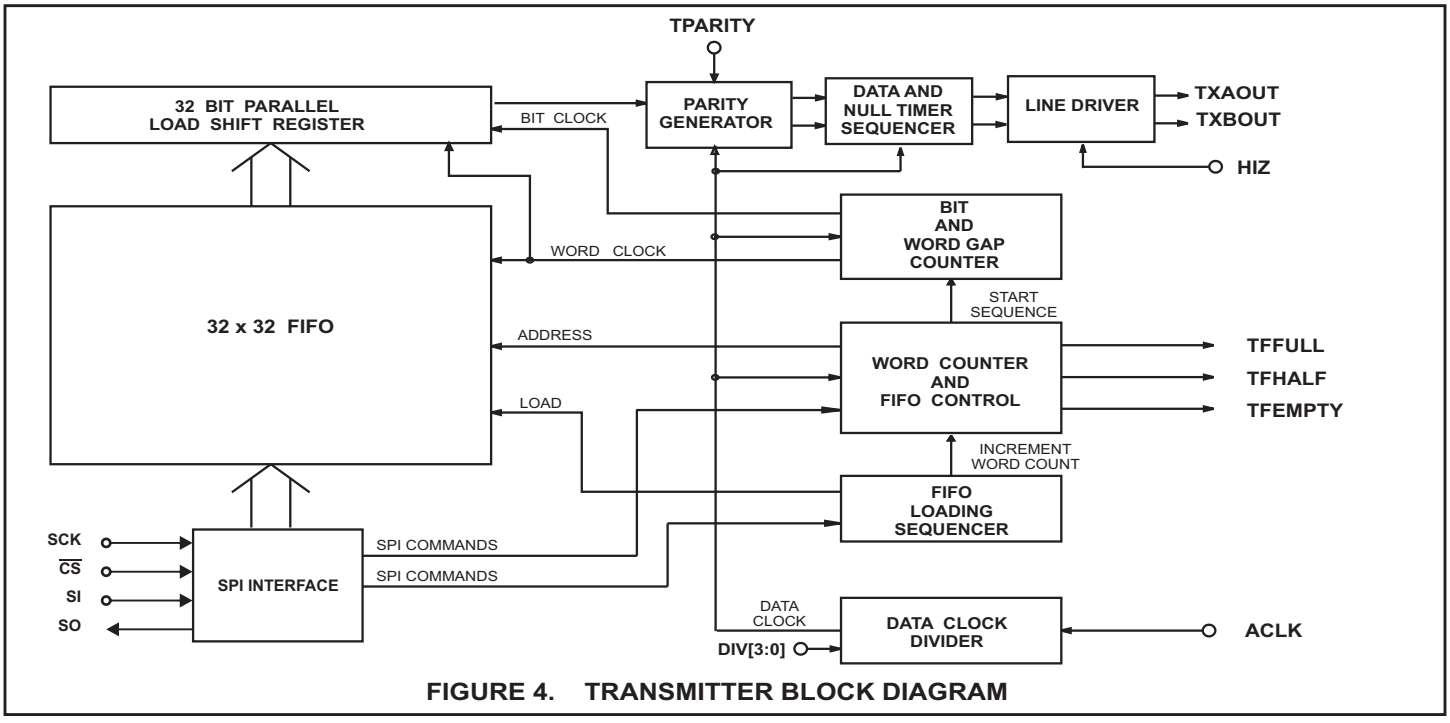


FIGURE 4. TRANSMITTER BLOCK DIAGRAM

SERIAL PERIPHERAL INTERFACE

SERIAL PERIPHERAL INTERFACE (SPI) BASICS

The HI-3593 uses an SPI synchronous serial interface for host access to internal registers and data FIFOs. Host serial communication is enabled through the Chip Select ($\overline{CS}$) pin, and is accessed via a three-wire interface consisting of Serial Data Input (SI) from the host, Serial Data Output (SO) to the host and Serial Clock (SCK). All read / write cycles are completely self-timed.

The SPI (Serial Peripheral Interface) protocol specifies master and slave operation; the HI-3593 operates as an SPI slave.

The SPI protocol defines two parameters, CPOL (clock polarity) and CPHA (clock phase). The possible CPOL-CPHA combinations define four possible "SPI Modes". Without describing details of the SPI modes, the HI-3593 operates in mode 0 where input data for each device (master and slave) is clocked on the rising edge of SCK, and output data for each device changes on the falling edge (CPHA = 0, CPOL = 0). Be sure to set the host SPI logic for mode 0.

As seen in Figure 5, SPI Mode 0 holds SCK in the low state when idle.

The SPI protocol transfers serial data as 8-bit bytes. Once $\overline{CS}$ chip select is asserted, the next 8 rising edges on SCK latch input data into the master and slave devices, starting with each byte's most-significant bit. The HI-3593 SPI can be clocked at 10 MHz.

Multiple bytes may be transferred when the host holds $\overline{CS}$ low after the first byte transferred, and continues to clock SCK in multiples of 8 clocks. A rising edge on $\overline{CS}$ chip select terminates the serial transfer and reinitializes the HI-3593 SPI for the next transfer. If $\overline{CS}$ goes high before a full byte is clocked by SCK, the incomplete byte clocked into the device SI pin is discarded.

In the general case, both master and slave simultaneously send and receive serial data (full duplex), per Figure 5 below. However the HI-3593 operates half duplex, maintaining high impedance on the SO output, except when actually transmitting serial data. When the HI-3593 is sending data on SO during read operations, activity on its SI input is ignored. Figures 6 and 7 show actual behavior for the HI-3593 SO output.

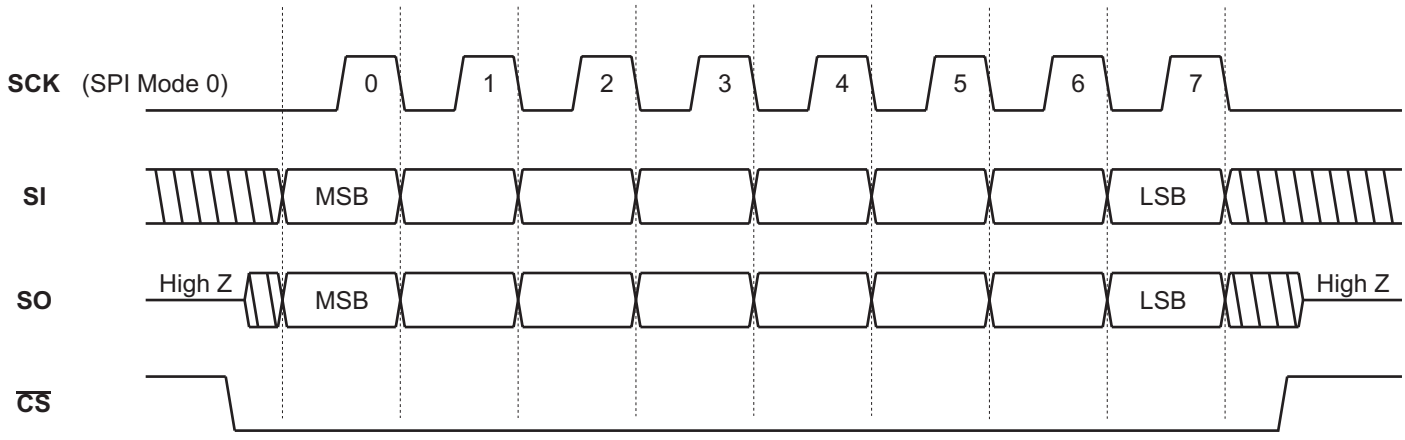


FIGURE 5. Generalized Single-Byte Transfer Using SPI Protocol Modes 0

HOST SERIAL PERIPHERAL INTERFACE, cont.

HI-3593 SPI COMMANDS

For the HI-3593, each SPI read or write operation begins with an 8-bit command byte transferred from the host to the device after assertion of $\overline{CS}$. Since HI-3593 command byte reception is half-duplex, the host discards the dummy byte it receives while serially transmitting the command byte.

Figures 6 and 7 show read and write timing as it appears for a single-byte and dual-byte register operation. The command byte is immediately followed by a data byte comprising the 8-bit data word read or written. For a single register read or write, $\overline{CS}$ is negated after the data byte is transferred.

Multiple byte read or write cycles may be performed by transferring more than one byte before $\overline{CS}$ is negated. Table 1. defines the required number of bytes for each instruction.

Note: SPI Instruction op-codes not shown in Table 1 are "reserved" and must not be used. Further, these op-codes will not provide meaningful data in response to read commands.

Two instruction bytes cannot be "chained"; $\overline{CS}$ must be negated after the command, then reasserted for the following Read or Write command.

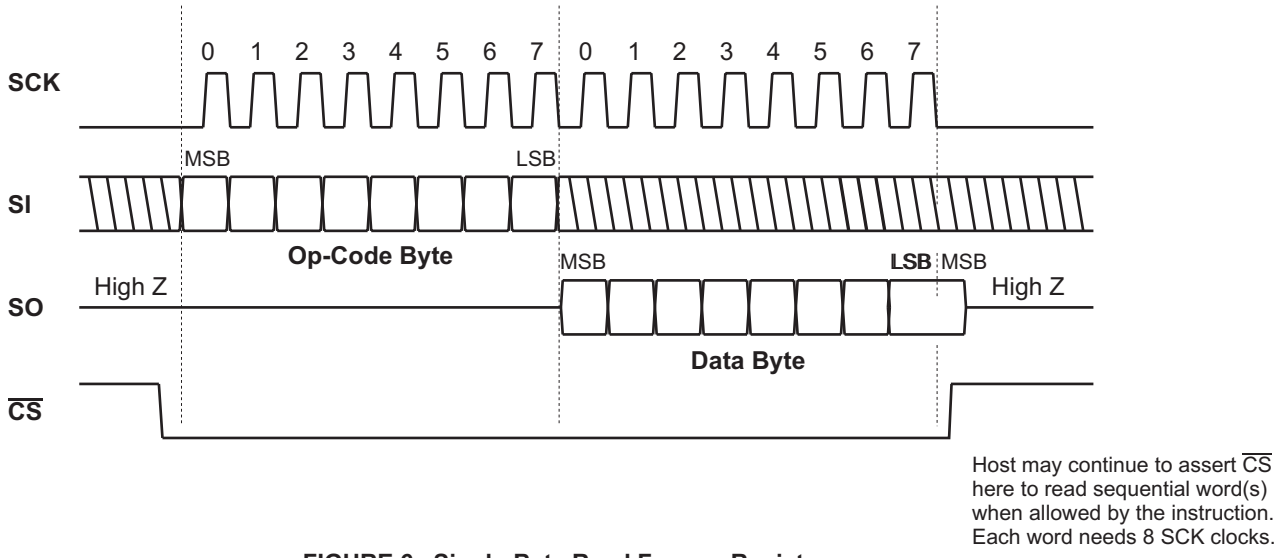


FIGURE 6. Single-Byte Read From a Register

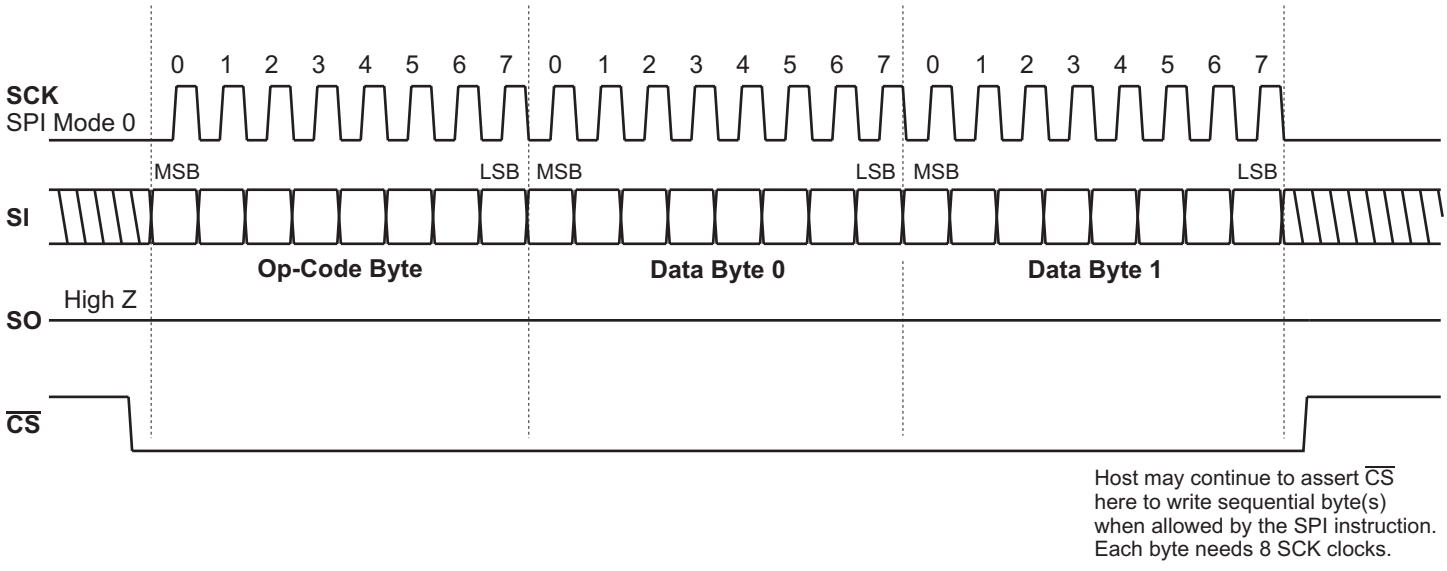
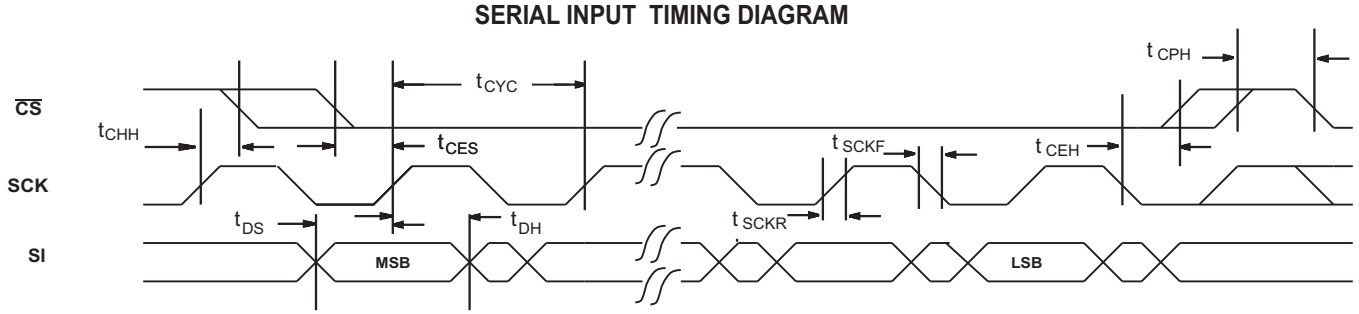


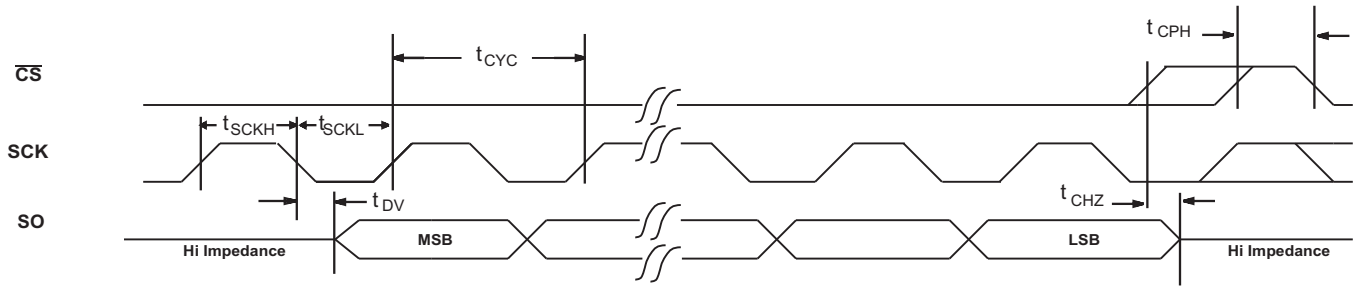
FIGURE 7. 2-Byte Write example

TIMING DIAGRAMS

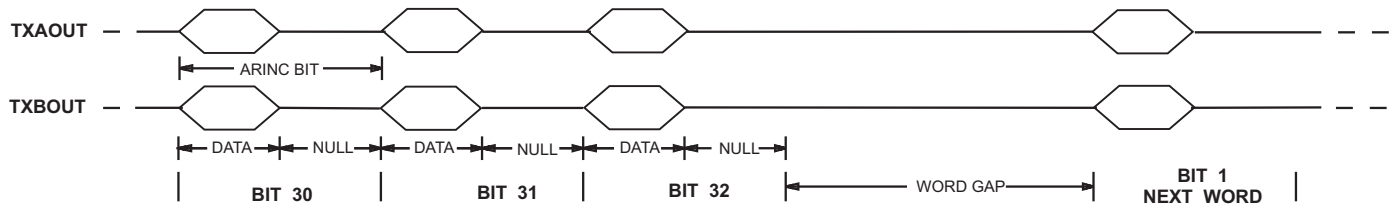
SERIAL INPUT TIMING DIAGRAM



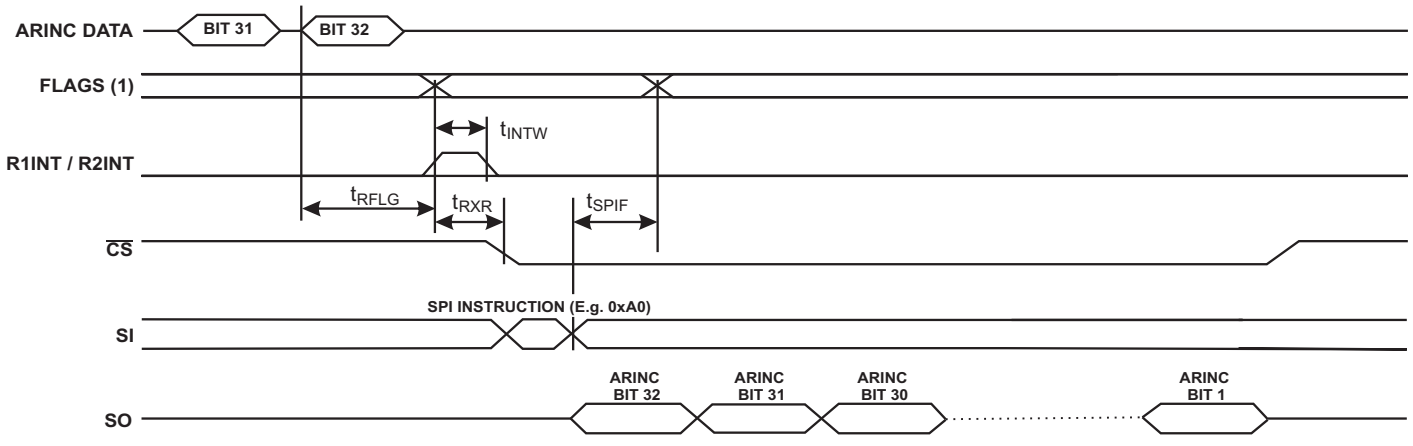
SERIAL OUTPUT TIMING DIAGRAM



DATA RATE - EXAMPLE PATTERN

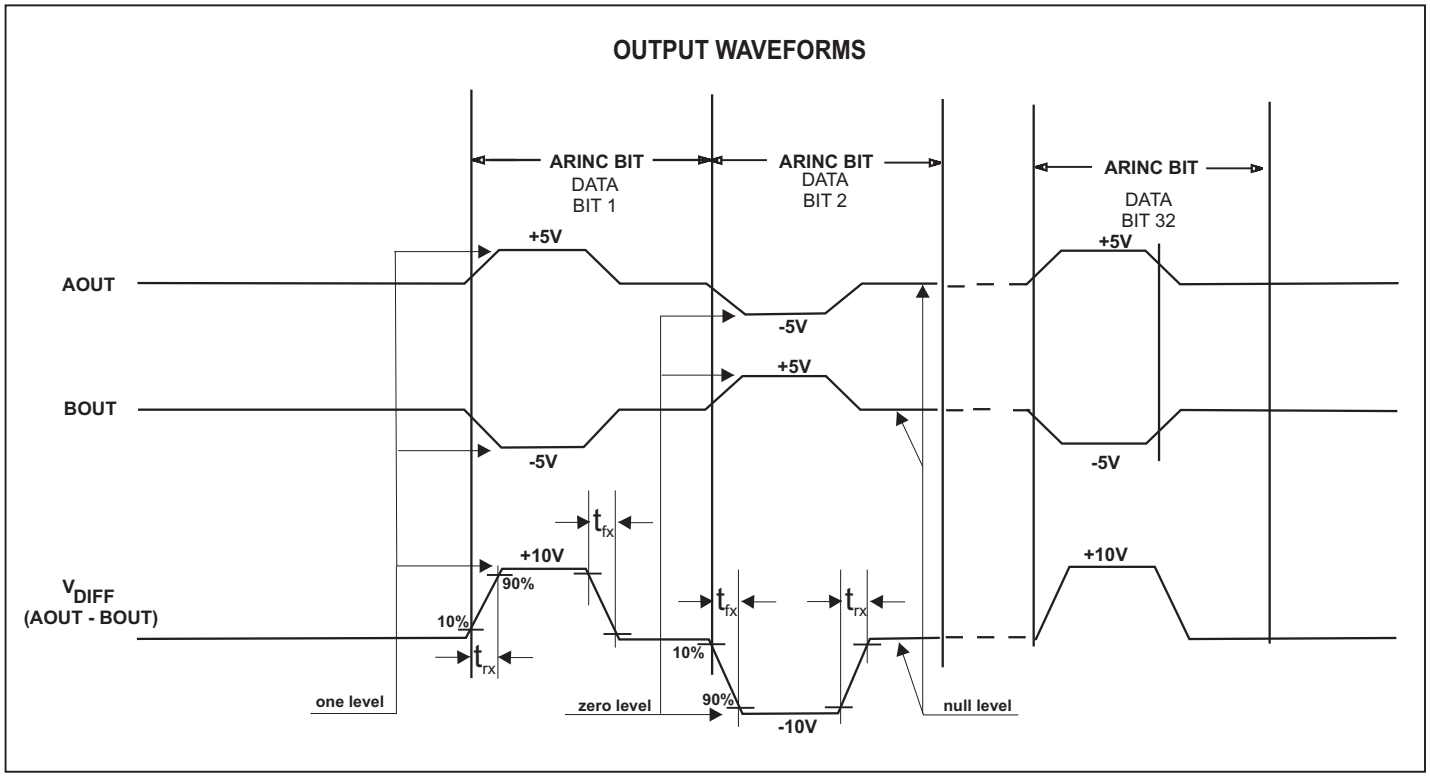


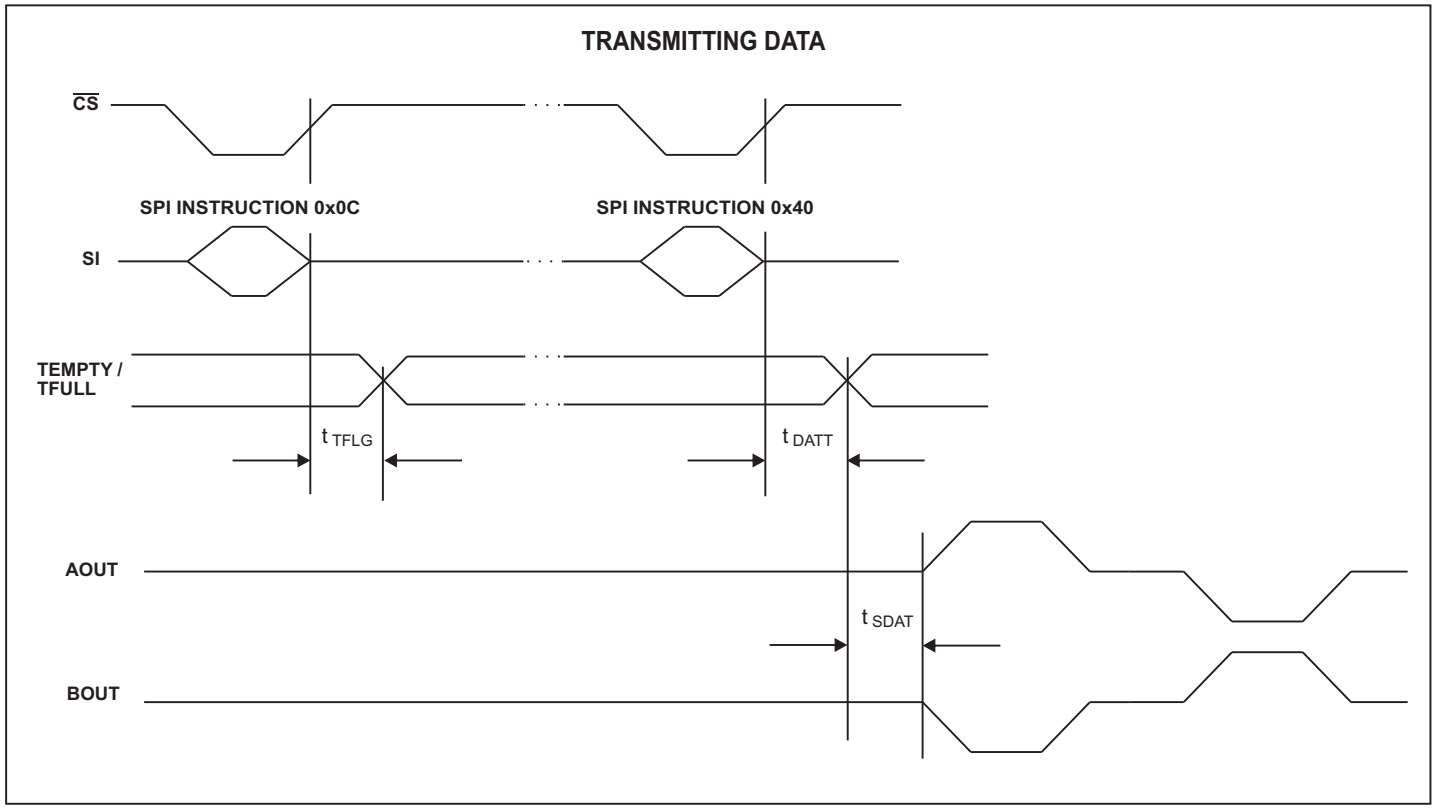
RECEIVER OPERATION



(1) Receiver status flag outputs: R1FLAG, R2FLAG, MB1-1, MB1-2, MB1-3, MB2-1, MB2-2, MB2-3

TIMING DIAGRAMS (cont.)

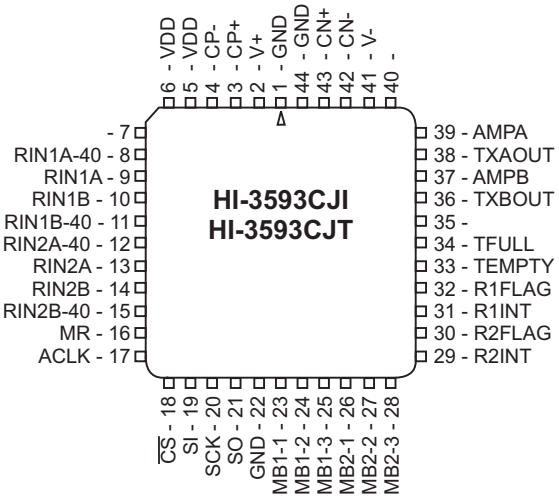




HEAT SINK - CHIP-SCALE PACKAGE ONLY

The HI-3593PCx uses a 44-pin plastic chip-scale package. This package has a metal heat sink pad on its bottom surface. This heat sink is electrically isolated from the die. To enhance thermal dissipation, the heat sink can be soldered to matching circuit board pad.

ADDITIONAL PACKAGE CONFIGURATIONS



44 - Pin J-LEAD CERQUAD

ABSOLUTE MAXIMUM RATINGS

Supply Voltages V_{DD} ..... -0.3V to +5.0V V+ ..... +7.0V V- ..... -7.0V	Power Dissipation at 25°C Plastic Quad Flat Pack ..... 1.5 W, derate 10mW/°C
Voltage at pins RINxx-xx ..... -120V to +120V	DC Current Drain per digital input pin ..... ±10mA
Voltage at pins TXAOUT, TXBOUT, AMPA, AMPB ..... V- to V+	Storage Temperature Range ..... -65°C to +150°C
Voltage at any other pin ..... -0.3V to V_{DD} +0.3V	Operating Temperature Range (Industrial): ..... -40°C to +85°C (Extended): ..... -55°C to +125°C
Solder temperature (Reflow)..... 260°C	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER		SYMBOL	CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
ARINC 429 INPUTS - Pins RIN1/2A, RIN1/2B, RIN1/2A-40 (with external 40KOhms), RIN1/2B-40 (with external 40KOhms)							
Differential Input Voltage:	ONE	V_{IH}	Common mode voltages	6.5	10.0	13.0	V
(RIN1A to RIN1B, RIN2A to RIN2B)	ZERO	V_{IL}	less than ±25V with	-13.0	-10.0	-6.5	V
	NULL	V_{NUL}	respect to GND	-2.5	0	2.5	V
Input Resistance:	Differential	R_I		-	140	-	KΩ
	To GND	R_G		-	140	-	KΩ
	To V_{DD}	R_H		-	100	-	KΩ
Input Current:	Input Sink	I_{IH}				200	µA
	Input Source	I_{IL}		-450			µA
Input Capacitance:	Differential	C_I	(RINxA to RINxB)			20	pF
(Guaranteed but not tested)	To GND	C_G				20	pF
	To V_{DD}	C_H				20	pF
LOGIC INPUTS							
Input Voltage:	Input Voltage HI	V_{IH}		80% VDD			V
	Input Voltage LO	V_{IL}				20% VDD	V
Input Current:	Input Sink	I_{IH}				1.5	µA
	Input Source	I_{IL}		-1.5			µA
	Pull-down Current (MR, SI, SCK, ACLK pins)	I_{PD}			60		µA
	Pull-up current ($\overline{CS}$ pin)	I_{PU}			-60		µA
ARINC 429 OUTPUTS - Pins TXAOUT, TXBOUT, (or AMPA, AMPB with external 32.5 Ohms)							
ARINC output voltage (Ref. To GND)	One or zero	V_{DOUT}	No load and magnitude at pin,	4.50	5.00	5.50	V
	Null	V_{NOUT}		-0.25		0.25	V
ARINC output voltage (Differential)	One or zero	V_{DDIF}	No load and magnitude at pin,	9.0	10.0	11.0	V
	Null	V_{NDIF}		-0.5		0.5	V
ARINC output current		I_{OUT}	Momentary short-circuit current	80			mA
LOGIC OUTPUTS							
Output Voltage:	Logic "1" Output Voltage	V_{OH}	I_{OH} = -100µA	90%VDD			V
	Logic "0" Output Voltage	V_{OL}	I_{OL} = 1.0mA			10% VDD	V
Output Current:	Output Sink	I_{OL}	V_{OUT} = 0.4V	1.6			mA
	Output Source	I_{OH}	V_{OUT} = V_{DD} - 0.4V			-1.0	mA
Output Capacitance:		C_O			15		pF
OPERATING VOLTAGE RANGE							
		V_{DD}		3.15		3.45	V
OPERATING SUPPLY CURRENT							
Transmitting Data in High-Speed Mode.		I_{DD}	Outputs Unloaded			50	mA
Transmitting Data in High-Speed Mode.		I_{DDL}	400 Ohm Differential Output Load			75	mA

AC ELECTRICAL CHARACTERISTICS

VDD = 3.3V, TA = Operating Temperature Range and fclk=1MHz ±0.1%

PARAMETER	SYMBOL	LIMITS			UNITS
		MIN	TYP	MAX	
SPI INTERFACE TIMING					
SCK clock period	t_{CYC}	100			ns
$\overline{CS}$ active after last SCK rising edge	t_{CHH}	10			ns
$\overline{CS}$ setup time to first SCK rising edge	t_{CES}	10			ns
$\overline{CS}$ hold time after last SCK falling edge	t_{CEH}	10			ns
$\overline{CS}$ inactive between SPI instructions	t_{CPH}	55			ns
SPI SI Data set-up time to SCK rising edge	t_{DS}	10			ns
SPI SI Data hold time after SCK rising edge	t_{DH}	10			ns
SCK rise time	t_{SCKR}			10	ns
SCK fall ime	t_{SCKF}			10	ns
SCK pulse width high	t_{SCKH}	20			ns
SCK pulse width low	t_{SCKL}	25			ns
SO valid after SCK falling edge	t_{DV}			35	ns
SO high-impedance after $\overline{CS}$ inactive	t_{CHZ}			30	ns
MR pulse width	t_{MR}	50			ns
RECEIVER TIMING					
Delay - Last bit of received ARINC word to Receive Flag change - Hi Speed	t_{RFLG}			16	µs
Delay - Last bit of received ARINC word to Receive Flag change - Lo Speed	t_{RFLG}			126	µs
Received data available to SPI interface. RxFLAG to $\overline{CS}$ active	t_{RXR}	0			ns
SPI receiver read FIFO instruction to RxFLAG	t_{SPIF}	0		t_{CYC}	ns
RxINT pulse width	t_{INT}		500		ns
TRANSMITTER TIMING					
SPI transmit data write (FIFO Flag Empty or Full)	t_{TFLG}			0	ns
FIFO Flag delay after enable transmit instruction - Hi Speed	t_{DATT}			2	µs
FIFO Flag delay to ARINC 429 data output - Hi Speed	t_{SDAT}			40	µs
FIFO Flag delay to ARINC 429 data output - Lo Speed	t_{SDAT}			320	µs
Line driver transition differential times:					
High Speed high to low	t_{fx}	1.0	1.5	2.0	µs
low to high	t_{rx}	1.0	1.5	2.0	µs
Low Speed high to low	t_{fx}	5.0	10	15	µs
low to high	t_{rx}	5.0	10	15	µs

CONVERTER CHARACTERISTICS

V_{DD} = +3.3V, T_A = Operating Temperature (unlesss otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Start-up transient (V+, V-)	t_{START}		-	-	10	ms
Operating Switching Frequency	f_{SW}		-	650	-	kHz
Worst case maximum voltage doubler output	$V_{DD2+(max)}$	V_{DD} = 3.6V, T= -55C, Open load	-		6.93	V
	$V_{DD2-(max)}$		-		-6.93	V
Capacitor Requirements (see block diagram on p. 2 for capacitor placement)						
V+ Fly-back capacitor, non-polarized	C_{FLY+}		0.47	-	-	µF
x7R MLCC, 10V minimum	$ESR_{(CFLY+)}$	500 kHz			500	mΩ
V- Fly-back capacitor, non-polarized	C_{FLY-}		2.2	-	-	µF
x7R MLCC, 10V minimum	$ESR_{(CFLY-)}$	500 kHz			500	mΩ
Two bulk storage capacitors, non-polarized	C_{OUT}		10	-	47	µF
X7R MLCC or tantalum, 10V minimum	$ESR_{(COUT)}$	500 kHz			300	mΩ
Supply de-coupling capacitors,	C_{SUPPLY}	Two parallel capacitors	-	0.1	-	µF
x7R MLCC or tantalum, 10V minimum			10		47	µF

ORDERING INFORMATION

HI - 3593 PQ x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No
M	-55°C TO +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PQ	44 PIN PLASTIC QUAD FLAT PACK, PQFP (44PMQS)

HI - 3593 PC x x

PART NUMBER	LEAD FINISH
Blank	NiPdAu
F	NiPdAu (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No
M	-55°C TO +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PC	44 PIN PLASTIC CHIP-SCALE, QFN (44PCS)

HI - 3593 CJ x (Ceramic)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
I	-40°C TO +85°C	I	No	Tin / Lead (Sn / Pb) Solder
T	-55°C TO +125°C	T	No	Tin / Lead (Sn / Pb) Solder

PART NUMBER	PACKAGE DESCRIPTION
CJ	44 PIN J-LEAD CERQUAD (44U)

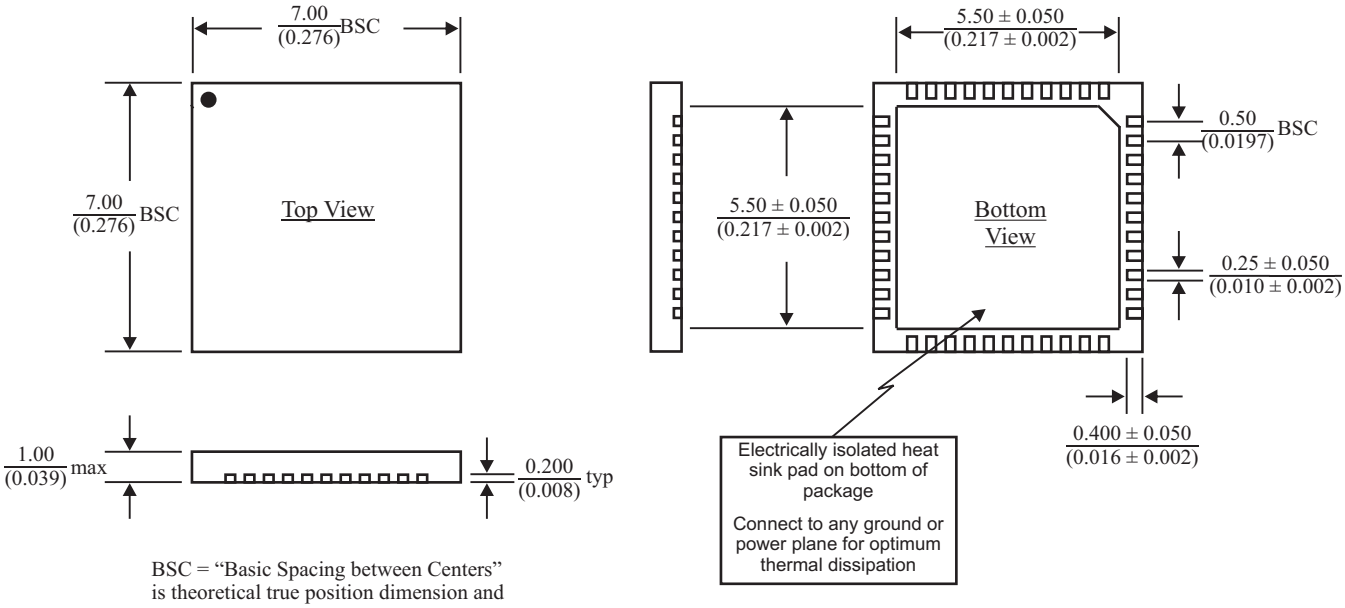
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS3593	NEW	02/03/08	Initial Release
	A	08/11/11	Modified AC Electrical Characteristics for 10 MHZ SPI operation.
	B	08/13/13	Updated DC/DC converter section. Added Converter Characteristics section to AC Electrical Characteristics. Corrected description for op codes 0x14 and 0x28 in Table 1. Clarified Solder Reflow Temperature. Update QFN and QFP package drawings.
	C	11/22/13	Update QFN-44 and PQFP-44 package drawings. Update converter characteristics table to match recommended capacitor values in AN-160.
	D	10/03/14	Update Converter Characteristics table and text description. Correct converter caps. ESR values from a “min.” to a max. value. Add C_{SUPPLY} caps. to block diagram.
	E	10/15/15	Clarify t_{CZH} timing parameter (SO high-impedance after $\overline{CS}$ inactive, not SCK falling edge).
	F	03/13/18	Add 44-Pin J-Lead Ceramic Quad Package. Correct typo in Ordering Information (PQ package designator should be PMQS, not PTQS)
	G	07/30/2020	Update QFN lead finish to NiPdAu. Update chassis ground symbols in block diagram to logic ground.

44-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 44PCS

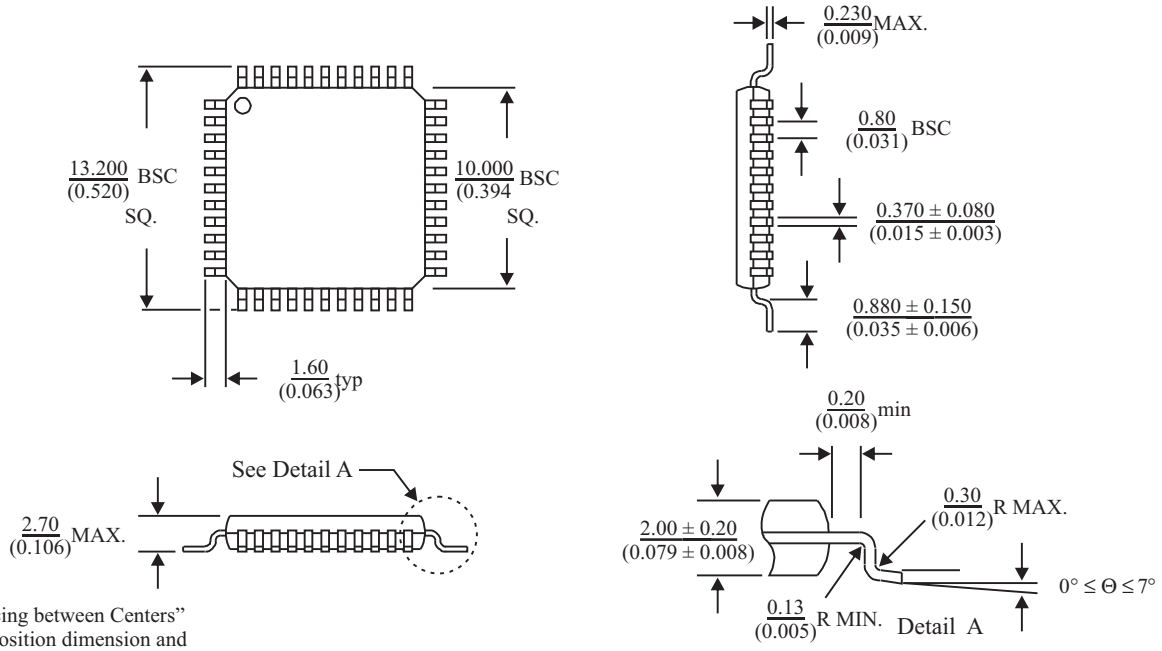


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 44PMQS

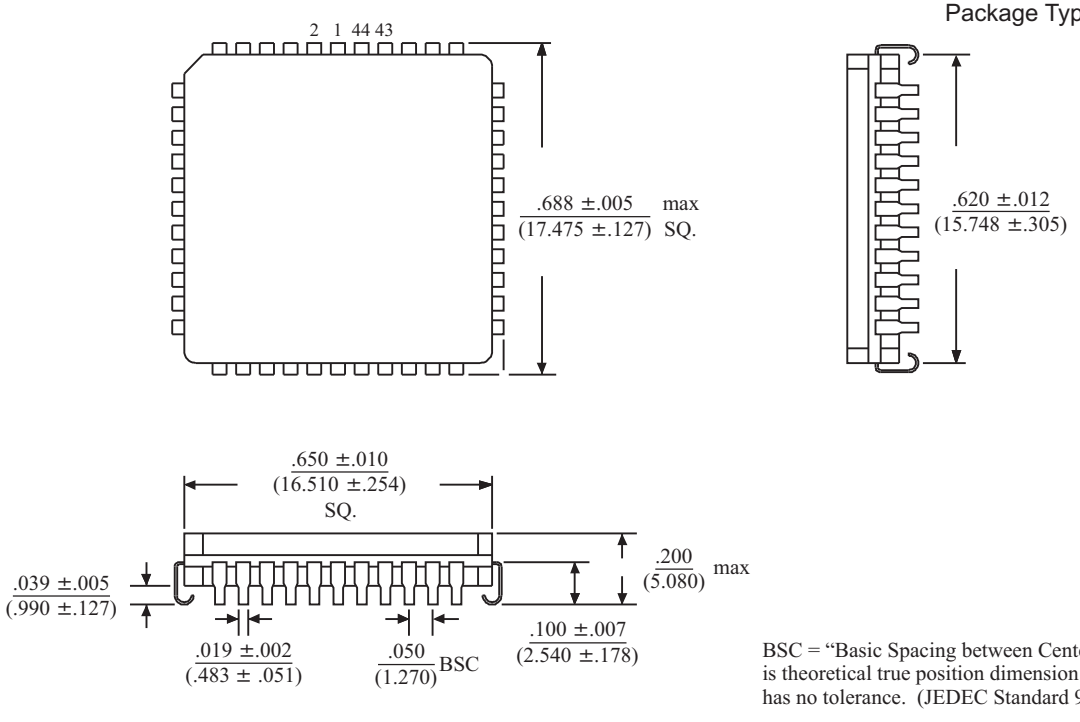


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN J-LEAD CERQUAD

inches (millimeters)

Package Type: 44U



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)